UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/636,181	08/07/2003	Andrei Mihnea	400.237US01	1762

27073 7590 09/20/2005

LEFFERT JAY & POLGLAZE, P.A.
P.O. BOX 581009
MINNEAPOLIS, MN 55458-1009

EXAMINER	
PHAM, LY D	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/636,181	MIHNEA ET AL.	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-14* is/are pending in the application.

4a) Of the above claim(s) *8-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL ACTION

DETAILED ACTION

1. Applicants' amendment filed August 29, 2005 has been entered. Claim 2 has been canceled. Claim 1 has been amended. Claims 8 – 14 have been withdrawn. Claims 15 – 21 have been canceled.

Claim Objections

2. Claims 5 and 6 are objected to because of the following informalities:

Claims 5 and 6 depend on the original filed claim 2, which has been canceled and incorporated into claim 1, but their dependencies have not been amended. Therefore, for the purpose of examination, claims 5 – 7 will be assumed to be depending from current claim 1. Appropriate correction is required.

Response to Arguments

2. Applicant's arguments filed August 29, 2005 have been fully considered but they are not persuasive.

With regards to the remarks, page 5, lines 3 – 8, applicants argue that the soft programming technique disclosed by Haddad et al. is not applicable to what is claimed in the method for recovery operation. The Office would like to assert that soft programming, or in some instance referred to as light programming, is one method well known in the art for recovering, or correcting over-erased memory cells. Soft

programming is more than merely programming the cells lightly. It has a generally recognized equivalent meaning for over-erased correction method, which helps bring the cells threshold voltage back to its intrinsic levels, which is slightly above ground (assuming the cells are N-type; and as for P-type, slightly below ground. See Chang et al., US Pat 5,909,392, col. 3, lines 9 – 12, and col. 7, line 54 – col. 8, line 29). Several additional teachings of such application include Wong in US Pat 6,160,739, col. 3, lines 16 – 20, which teaches "touch-up" programming for tightening the erased threshold voltage Vt distribution to correct "over-erased" problem. Also, in US Pat 6,381,177, col. 1, line 55 – col. 2, line 10, De Sander et al. clearly teach the soft programming operation following an erasing operation to recover depleted cells—cells which have been over-erased. And in fact, Haddad et al. have clearly taught the programming operation for over-erase correction following an erase operation (col. 3, line 20 – col. 5, line 22), this programming operation for over-erase correction later referred to as soft programming (col. 5, lines 25 – 40), which again, perpetrates to tighten the threshold distribution by increasing the threshold voltage of the cells with the lowest threshold voltage.

As an additional emphasis, in contrary to applicant's remarks page 5, lines 9 – 16, the Office also want to point out what might have been a confusion per Mehrad is the difference between what soft programming serves, versus which soft programming connection technique that offers an extended life time as compared to the soft programming method taught in the prior art. Regardless, col. 1, line 47 – col. 2, line 9, col. 2, lines 58 – 61, and col. 5, lines 49 – 55 clearly teach the soft programming method for recovering over-erased cells from depletion.

In essence, the problem with memory cells being over-erased has been widely encountered in the art (as also pointed out in the application's invention background), in which case, the induced threshold voltage of the over-erased cells are very low, in some case, even negative (Haddad et al., col. 3, lines 41 – 64 and col. 4, lines 61 – 65). As a result, an obvious approach to correct, or to recover such over-erased cells is to somehow, bring the threshold voltage back up to some acceptable values (Haddad et al., col. 4, lines 11 – 14), which also appears agreeing to the applicants' approach (paragraph 0024).

In conclusion, the Office would like to make clear that so long there is a method for increasing the threshold voltage of a memory cell found to be over-erased, such method is recognized as an over-erased correction, regardless of its nomenclature, i.e., "soft-programming", "light programming, or even "recovery operation".

The foregoing establishes grounds on which the pending claims are viewed below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US Pat 5,909,392).

Regarding **claims 1, 5, and 6**, Chang et al. disclose a method for erasing a non-volatile PMOS floating gate memory cells block comprising a plurality of memory cells each having a gate input and two source/drain regions, the method comprising:

erasing the memory block (col. 7, lines 41 – 53, "page mode erase" erases a block of cells in an entire row); and

performing a recovery operation on the plurality of memory cells (abstract, soft-programming mechanism is used to compensate for over-erasing of the memory cells, and col. 8, lines 18 – 29, "Preferably, this soft-program operation is performed immediately after completion of an erasing operation") such that a threshold voltage indicating a programmed state, for over-erased cells, is increased (col. 7, lines 54 – 62, "it is necessary to return the threshold voltages V_T of the over-erased cells to between –1.5 and –2.0 volts" from a voltage more negative than –2 volts) by coupling the gate input to a ramped voltage (col. 8, lines 13 – 17), a first source/drain region to a first constant voltage (see figs. 2 and 3, and col. 7, line 66 – col. 8, line 13. "..., couples the p+ source 36 of the selected cell 30a(1) to the well potential line WP0, i.e., to **approximately 9 volts—first constant voltage**. Note that from fig. 2, the p+ source 36 is the bottom source/drain region of a memory cell in fig. 3, particularly in this instance, memory cell 30a(1)), and the remaining source/drain region to a second constant voltage (since the select gate line SG0 is grounded, which turns on the string select transistor 64a on, which then couples the bit line BL0 potential, held at between 0 – 2 volts to soft program cell 30a(1), to the top source/drain region of cell 30a(1) to some constant voltage near **between 0 – 2 volts—second constant voltage**).

Although Chang et al. did not clearly specify the erasing method for a nitride read only memory (NROM) block, however, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to utilize such method for the similar memory cell type, as NROM might be the case being provided for the purpose of reducing power consumption (col. 8, lines 39 – 47).

5. Claim 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US Pat 5,909,392) in view of Chung (US Pat Pub 2004/0185619 A1).

Regarding **claim 7**, though Chang et al. did not further teach the method of claim 1, wherein the NROM block be embedded in a CMOS device, the feature is however taught by Chung (paragraph 0008, lines 1 – 3). Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine the feature taught by Chung to the disclosure by Chang et al., to allow for further minimization of device size and increased device density without degradation in performance (paragraph 0008, lines 3 – 14).

6. Claims 1, 5 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (US Pat 6,598,752 B1) in view of Chung (US Pat Pub 2004/0185619 A1).

Regarding **claims 1, 5, and 6**, Hsu et al. disclose a method for erasing a nonvolatile NOR type EEPROM memory comprising:

erasing the memory block (fig. 4A, or abstract);

performing a recovery operation on the plurality of memory cells such that a threshold voltage indicating a programmed state for over-erased cells is increased (col. 7, lines 35 – 42, fig. 8 shows increasing threshold voltage Vt of over-erased cells at each .5V step) by coupling the gate input to a ramped voltage (step-ramped control gate voltage Vg), a first source/drain region to a first constant voltage (drain voltage set to 4.5 or 5 Volts, which is in a range of 3 – 7 volts), and the other source/drain region to a second constant voltage (col. 7, lines 18 – 19, "In the selected block 0, the source lines SL(0) is set to 0 Volt...". According to fig. 5, the source line SL(0) is connected to the other source/drain region of the memory cell, which means the second constant voltage is in the range of 0 – 3 volts).

Although Hsu et al. did not clearly show the erasing method for a nitride read only memory (NROM) block, however, advantages of application of nonvolatile NROM has been taught by Chung (paragraph 0006). Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the feature taught by Chung to the disclosure by Hsu et al., so that the ONO structure may be used to replace the gate dielectric used in floating gate devices (paragraphs 0007 and 0009).

As per **claim 7**, Chung also discloses the method of claim 1, wherein the NROM memory cell is embedded in a CMOS device (paragraph 0008).

7. Claims 1 – 4, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haddad et al. (US Pat 6,172,909 B1) in view of Chung (US Pat Pub 2004/0185619 A1).

Regarding **claims 1 and 2**, Haddad et al. disclose a method for erasing a EEPROM block comprising a plurality of memory cells (fig. 1A) each having a gate input (fig. 1, gates connected to word lines) and two source/drain regions (fig. 1, one connected to the source line to the power source 106, and the other connected to bit line to bit line driver 102), the method comprising:

erasing the memory block (col. 3, lines 7 – 19); and

performing a recovery operation after erasing the memory block of the plurality of memory cells such that a threshold voltage indicating a programmed state, for over-erased cells, is increased (abstract: soft programming for over-erased cells..., and col. 5, lines 25 – 40), the recovery operation includes biasing each of the plurality of memory cells with a ramped voltage on the gate input (col. 5, lines 41 – 45), a constant voltage on a first source/drain region and the remaining source/drain to a second constant voltage (abstract).

Although Haddad et al. did not clearly refer the EEPROM block as a NROM, as claimed in claim 1, however, the feature has been shown by Chung (paragraph 0010). Therefore, it is considered obvious to one of ordinary skill in the art, at the time the invention was made, to utilize the NROM in corporation with the disclosure by Haddad et al. for the advantages disclosed by Chung (paragraphs 0006 – 0009).

Regarding **claim 3**, Haddad et al. also disclose the method of claim 1, wherein the ramped voltage applies to the gate Is in a range of 0V to 3V (abstract: Vgs < 3V).

Regarding **claim 4**, Haddad et al. also disclose the method of claim 1, wherein the ramp voltage has a time period in a range of 10us to 1sec from start to end (col. 10, lines 44 – 47, '... <200msec in addition to the typical 0.5 to 1.0 second erase time per sector').

As per **claim 7**, Chung further disclose the NROM embedded in a CMOS device (paragraph 0009).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly D Pham
September 14, 2005

HUAN HOANG
PRIMARY EXAMINER